

Manolis G.H. Katevenis

Detailed Curriculum Vitae

last updated: 20 April 2011

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Areas of Interest:

- Scalable Multicore Systems: Interprocessor Communication and Memory Architecture;
- Interconnection Network Architecture; Packet Switch Architecture;
- Computer Architecture; VLSI Systems.

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1. Positions Held, Education, Awards, Biography

last updated: 20 April 2011

1.1 Positions Held:

Academic:

- **1996 - :** Professor, Computer Science Department ([CSD](#)), University of Crete ([UoC](#)), Heraklion, Crete, Greece
- Chairman, Computer Science Department, University of Crete, Heraklion, Crete, Greece (**1994-96** and **1998-2000**)
- Associate Professor, Computer Science Department, University of Crete, Heraklion, Crete, Greece (**1992 - 1995**)
- Assistant Professor, Computer Science Department, University of Crete, Heraklion, Crete, Greece (**1986 - 1991**)
- Assistant Professor, Dept. of Computer Science, [Stanford University](#), Stanford, California, USA (**1984 - 1985**)

Research:

- **1986 - :** Head, Computer Architecture and VLSI Systems ([CARV](#)) Laboratory, Institute of Computer Science ([ICS](#)), Foundation for Research and Technology - Hellas ([FORTH](#)) Heraklion, Crete, Greece (In the 80's, FORTH was called "Research Center of Crete", and CARV was called "Hardware Lab"; in the early 90's, CARV was called "Architecture and VLSI Group")
- **2005 - :** Deputy Director, Institute of Computer Science, FORTH

- **2004 -** : European Network of Excellence on High-Performance and Embedded Architecture and Compilation ([HiPEAC](#)): founding partner, member of the Steering Committee, and coordinator of Interconnection Networks Architecture

Management, Visiting:

- Member of the Board of Directors, Nanochronous Logic Inc., San Jose, California, USA (**2007 - 2010**) (spin-off company of FORTH-ICS)
- National Representative of Greece, ARTEMIS mirror group, European Commission (**2006 and 2007**)
- National Representative of Greece, ESPRIT Management Committee (ITC), European Commission (**1994 - 1998**)
- Visiting Faculty, Computer Science Division - EECS, University of California, Berkeley, CA USA (**1997** Fall Semester)
- Sabbatical at the Advanced Computer Research Institute (ACRI) S.A., Lyon, France (**1991** Fall Semester)
- Visiting Faculty, Department of Computer Science, Stanford University, Stanford, California, USA (**1987** Fall Semester)

1.2 Education:

- Ph.D. in Computer Science, University of California, Berkeley, CA USA (**1983**). Thesis: *Reduced Instruction Set Computer Architectures for VLSI*; Advisors: David Patterson and Carlo Sequin.
- MSc. in Electrical Engineering and Computer Science, University of California, Berkeley, CA USA (**1980**).
- Diploma of Electrical Engineering, National Technical University of Athens (NTUA), Greece (**1978**).

1.3 Awards:

- Award by the Secretary General of the Region of Crete **2003** - jointly with Stelios Orphanoudakis and Panos Constantopoulos - as the Principal Organizers of the Department of Computer Science, University of Crete.
- [ACM Doctoral Dissertation Award](#) **1984** ``For his dissertation "Reduced Instruction Set Computer Architectures for VLSI."''
- [David J. Sakrison Memorial Prize](#) **1983** - jointly with Robert Sherburne, Jr. - University of California, Berkeley.
- IBM PhD Fellowship, **1981 - 1983**, while a graduate student at the University of California, Berkeley.
- Greek State Fellowship, **1973 - 1978**, while an undergraduate student at NTUA.

1.4 Brief Biography:

Manolis G.H. Katevenis received his Ph.D. degree in Computer Science from the University of California, Berkeley, in 1983. From January 1984 to March 1985 he was Assistant Professor of Computer Science at Stanford University, Stanford, California, USA. Since September 1985, he is with the *University of Crete*, Dept. of Computer Science, where he is currently a Professor; according to an Award by the Secretary General of the Region of Crete in 2003, Katevenis is recognized as one of the three Principal Organizers of this Department. Since 1985, he is also with the *Institute of Computer Science (ICS)*, FORTH, Heraklion, Crete, where he is currently Deputy Director, and the Head of the *Computer Architecture and VLSI Systems Laboratory*. In 2003-2004, he was a founding partner of [HiPEAC](#), the European Network of Excellence on High-Performance and Embedded Architecture and Compilation, where he is now a member of the Steering Committee and coordinator of Interconnection Networks Architecture.

His interests are in: Scalable Multicore Systems - Interprocessor Communication and Memory Architecture; Interconnection Network Architecture; Packet Switch Architecture; Computer Architecture; and VLSI Systems.

During his doctoral studies (1980-83), he was the chief implementor of the *RISC II* single-chip microprocessor at U.C.Berkeley (precursor of the SUN SPARC architecture), and for this [thesis](#) he received the 1983 [Sakrison Memorial Prize](#) and the 1984 [ACM Doctoral Dissertation Award](#). The RISC ideas revolutionized the microprocessor industry in the late 80's. After Berkeley, he consulted for AMD during the design of the "AMD-29000" RISC microprocessor, for Daisy Systems during the design of a hardware accelerator, for two other companies during the design of very-high speed RISC processors in ECL and GaAs, for a Storage Area Networking (SAN) company, and for DEC, SRC, where he did the preliminary switch design for "Autonet", precursor of DEC's "ATM GigaSwitch". In 1987, during the first meetings of the IEEE Standard 1596-1992 Scalable Coherent Interface (SCI) Committee, he was the first to propose using point-to-point connections rather than a bus architecture.

In 1985-91, he made pioneering contributions in per-flow queueing, backpressure, congestion tolerance, and weighted round-robin scheduling, yielding weighted max-min fairness in switches for high speed networks --topics whose industrial application is seen one or two decades later. In 1991-92, he worked on switch design for multiprocessor interconnection networks. In 1996-98, Katevenis was the technical leader of the design of *ATLAS I*, a 6-million-transistor single-chip 16x16 ATM switch, implemented in 0.35-micron CMOS, featuring 10 Gb/s throughput, sub-microsecond cut-through latency, and credit-based flow control (backpressure) at the granularity of 32 thousand virtual channels. In 1998-2001, he introduced *wormhole IP over ATM*, and led the design of pipelined heap management for schedulers in multi-gigabit weighted fair queueing, and hardware for managing thousands of queues in DRAM at 10 Gb/s line rate. In 2002-2005, his research concerned the architecture of and congestion management in non-blocking switching fabrics with internal backpressure, and distributed scheduling in buffered crossbars. In 2006-2011, he worked on networks-on-chip (NoC), including the micro-architecture of high-radix on-chip crossbar switches.

Katevenis' work on parallel processing started in 1993-95, when he led the *Telegraphos* project in ICS-FORTH, where workstation clustering prototypes were designed and built, based on remote-write, remote-DMA, and remote-enqueue operations, including processor-network interfaces for protected user-level communication. Since 2006, his research concerns interprocessor communication and memory architecture in on-chip and system-wide embedded and scalable multi-processor systems. In the *SARC* project, he led the design of an architecture and FPGA prototype that unifies explicit and implicit communication by integrating the network interface with the cache controller, basing their common operation on a configurable event-response hardware mechanism.

For more information, see: <http://www.ics.forth.gr/~kateveni>

2. Publications

last updated: 20 April 2011

According to "Harzing Publish or Perish v.3.0.3813", run on 14 April 2011, with Query: "Katevenis from 1970 to 2011: all":

Papers: 100; Citations: 1597; h-index: 20; AWCR: 106.14; Cites/paper: 15.97; Cites/author: 971.34; g-index: 38; AW-index: 10.30; Years: 32; Papers/author: 54.78; hc-index: 12; AWCRpA: 57.77; Cites/year: 49.91; Authors/paper: 2.21; hI-index: 9.76; e-index: 30.33; hI_norm: 13; hm-index: 13.33; Hirsch: a=3.99, m=0.63; Contemporary ac=2.95; Cites/paper: 15.97/3.0/0 (mean/median/mode); Authors/paper: 2.21/2.0/2 (mean/median/mode). 22 papers with 1 author; 46 papers with 2 authors; 22 papers with 3 authors; 9 papers with 4 authors; 1 paper with 5 authors.

2.1 Books, Edited Books, Translated Books:

B4

M. Katevenis, M. Martonosi, C. Kozyrakis, O. Temam, T. Ungerer (Eds.): *Proceedings of the 6th International Conference on High Performance and Embedded Architectures and Compilers - HiPEAC 2011*, ACM Digital Library, ISBN: 978-1-4503-0241-8, Heraklion, Crete, Greece, 24-26 January 2011, 223 pages.

B3

P. Stenstrom, M. Dubois, M. Katevenis, R. Gupta, T. Ungerer (Eds.): *Proceedings, Third International Conference on High Performance Embedded Architectures and Compilers - HiPEAC 2008*, Goteborg, Sweden, Jan. 2008, 400 pages; LNCS 4917, Springer, ISSN 0302-9743, ISBN 978-3-540-77559-1.

B2

M. Mano: "*Digital Design*", Prentice-Hall, 1984, ISBN 0-13-212333-9. **Greek translation** by M. Katevenis with the assistance of a group of graduate students, Technical Chamber of Greece Editions, **1986**, 592 pages.

B1

M. Katevenis: "*Reduced Instruction Set Computer Architectures for VLSI*", 1984 [ACM Doctoral Dissertation Award](#), MIT Press, ISBN 0-262-11103-9, **1985**.

2.2 Book Chapters (full-text reviewed):**BC4**

S. Kavadias, M. Katevenis, D. Pnevmatikatos: "Network Interface Design for Explicit Communication in Chip Multiprocessors", Chapter 10 in the book: *Designing Network-on-Chip Architectures in the Nanoscale Era*, J. Flich and D. Bertozzi (Eds.), CRC Press - Taylor & Francis Groupa, ISBN: 978-1-4398-3710-8, **2011**, pp. 325-351.

BC3

M. Katevenis: "*RISC Architectures*", Chapter 20 in the book: *Parallel and Distributed Computing Handbook*, A. Zomaya Ed., McGraw-Hill, ISBN 0-07-073020-2, **1995**, pp. 594-619.

BC2

M. Katevenis: "*The Nature of General-Purpose Computations*", Chapter 2 (pp. 13-34) in the book: *Reduced Instruction Set Computers*, W. Stallings, Editor, IEEE Computer Society Press Tutorial, 2nd Edition, ISBN 0-8186-8943-9, **1990**.

BC1

M. Katevenis, C. Sequin, D. Patterson, R. Sherburne: "*RISC: Effective Architectures for VLSI Computers*", Chapter 2 in the book: *VLSI Electronics: Microstructure Science - Vol. 14: VLSI Design*, N. Einspruch, Editor, Academic Press, ISBN 0-12-234114-7, **1986**, pp. 36-77.

2.3 Patents, Patent Applications:**PA3**

E. Markatos, M. Katevenis, P. Vatsolaki: "*Notification of Message Arrival in a Parallel Computer System*", Foundation for Research and Technology -- Hellas (FORTH), Heraklion Crete Greece, *European Patent Application No. 97410036.4-2201*, 19 March **1997** (the Remote Enqueue operation).

PA2

M. Katevenis: "*A High-Throughput Data Buffer*", Foundation for Research and Technology -- Hellas (FORTH), Heraklion Crete Greece; issued *USA Patent Number 5,774,653*, 30 June 1998 (European Patent Application No. 95410074.9, 27 July 1995; Greek Patent Application No. 940100383, 2 Aug. **1994**) (Pipelined Memory Shared Buffer for Switching).

PA1

M. Katevenis: "*A Method for Operating a Computer with Binary Code Not Adapted Thereto*", ACRI S.A., Lyon, France, *European Patent Application No. 92/420162.7*, 18 May **1992** (on-the-flight binary translation from a foreign to the local instruction set).

2.4 Journal Publications - full-text reviewed:**J18**

N. Chrysos, M. Katevenis: "Distributed WFQ scheduling converging to weighted max-min

fairness", **Computer Networks** (Elsevier), ISSN 13891286, vol. 55, issue 3, Oct. **2010** (online), Feb. 2011 (in print), pp. 792-806.

J17

M. Katevenis, V. Papaefstathiou, S. Kavadias, D. Pnevmatikatos, F. Silla, D. Nikolopoulos: "Explicit Communication and Synchronization in SARC", **IEEE Micro**, vol. 30, no. 5, pp. 30-41, Sep./Oct. **2010**.

J16

D. Simos, I. Papaefstathiou, M. Katevenis: "Building an FoC Using Large, Buffered Crossbar Cores", **IEEE Design & Test**, vol. 25, no. 6, Nov. **2008**.

J15

A. Ioannou, M. Katevenis: "Pipelined Heap (Priority Queue) Management for Advanced Scheduling in High Speed Networks", **IEEE/ACM Transactions on Networking (ToN)**, vol. 15, no. 2, pp. 450-461, April **2007**.

J14

G. Sapountzis, M. Katevenis: "Benes Switching Fabrics with O(N)-Complexity Internal Backpressure", **IEEE Communications Magazine** vol. 43, no. 1, pp. 88-94, January **2005**.

J13

E. Markatos, D. Pnevmatikatos, M. Flouris, M. Katevenis: "Web-Conscious Storage Management for Web Proxies", **IEEE/ACM Transactions on Networking (ToN)**, vol. 10, no. 6, pp. 735-748, Dec. **2002**.

J12

M. Katevenis, Iakovos Mavroidis, G. Sapountzis, E. Kalyvianaki, Ioannis Mavroidis, G. Glykopoulos: "Wormhole IP over (Connectionless) ATM", **IEEE/ACM Transactions on Networking (ToN)**, vol. 9, no. 5, pp. 650-661, October **2001**.

J11

M. Katevenis, E. Markatos, P. Vatsolaki, C. Xanthaki: "The Remote Enqueue Operation on Networks of Workstations", *Informatica - an International Journal of Computing and Informatics*, ISSN 0350-5596, 23(1), pp. 29-39, April **1999**.

J10

G. Kornaros, D. Pnevmatikatos, P. Vatsolaki, G. Kalokerinos, C. Xanthaki, D. Mavroidis, D. Serpanos, M. Katevenis: "ATLAS I: Implementing a Single-Chip ATM Switch with Backpressure", **IEEE Micro**, vol. 19, no. 1, pp. 30-41, Jan/Feb. **1999**.

J9

D. Serpanos, M. Katevenis, E. Spyridakis: "ATLAS I: Building Block for ATM Networks with Credit-based Flow Control", *IEICE Trans. on Communications*, Japan, **1998**.

J8

M. Katevenis, D. Serpanos, G. Dimitriadis: "ATLAS I: A Single-Chip, Gigabit ATM Switch with HIC/HS Links and Multi-Lane Back-Pressure", *Microprocessors and Microsystems*, Elsevier, March **1998**.

J7

M. Katevenis, E. Markatos, G. Kalokerinos, A. Dollas: "Telegraphos: A Substrate for High Performance Computing on Workstation Clusters", *Journal of Parallel and Distributed Computing (JPDC)*, Academic Press, vol. 43, no. 2, pp. 94-108, June **1997**.

J6

M. Katevenis, P. Vatsolaki, V. Chalkiadakis: "Credit-Flow-Controlled ATM over HIC Links in the ASICCOM "ATLAS I" Single-Chip Switch", *Real-Time Magazine*, vol. 96, no. 3, pp. 65-72, July **1996**.

J5

M. Katevenis, S. Sidiropoulos, C. Courcoubetis: "Weighted Round-Robin Cell Multiplexing in a General-Purpose ATM Switch Chip", *IEEE Journal on Selected Areas in Communications (JSAC)*, Vol. 9, No. 8, pp. 1265-1279, October **1991**.

J4

M. Katevenis: "Fast Switching and Fair Control of Congested Flow in Broad-Band Networks", *IEEE Journal on Selected Areas in Communications (JSAC)*, Vol. 5, No. 8, pp. 1315-1326, October **1987**.

J3

R. Sherburne, M. Katevenis, D. Patterson, C. Sequin: "A 32-Bit NMOS Microprocessor with a Large Register File", *IEEE Journal of Solid State Circuits (JSSC)*, October **1984**.

J2

M. Katevenis, R. Sherburne, D. Patterson and C. Sequin: "The RISC II Micro-Architecture", *Journal of VLSI and Computer Systems*, Computer Science Press Inc., Vol. 1, No. 2, **1984**.

J1

D. Fitzpatrick, J. Foderaro, M. Katevenis, H. Landman, D. Patterson, J. Peek, Z. Peshkess, C. Sequin, R. Sherburne, K. VanDyke: "A RISCy Approach to VLSI", *VLSI Design Magazine*, Vol. II, No. 4, 4th qu. **1981**, pp. 14-20.

2.5 Conference and Major Workshop Proceedings Publications - full-text reviewed:

C48

Yanping Gao, C. Kachris, M. Katevenis: "An Efficient Sequential Iterative Matching Algorithm for CIOQ Switches", Proc. of the *16th IEEE Symposium on Computers and Communications (ISCC 2011)*, Kerkyra (Corfu), Greece, 28 June - 1 July 2011, 6 pages.

C47

G. Passas, M. Katevenis, D. Pnevmatikatos: "VLSI Micro-Architectures for High-Radix Crossbar Schedulers", Proc. of the *5th ACM/IEEE Int. Symposium on Networks-on-Chips (NOCS 2011)*, ISBN 978-1-4503-0720-8, Pittsburgh, PA, USA, 1-4 May 2011, 8 pages.

C46

P. Tendulkar, V. Papaefstathiou, G. Nikiforos, S. Kavadias, D. Nikolopoulos, M. Katevenis: "Fine-Grain OpenMP Runtime Support with Explicit Communication Hardware Primitives", Proc. of the *Design, Automation, and Test in Europe Conference (DATE 2011)*, ISBN: 978-3-9810801-7-9, Grenoble, France, 14-18 March 2011, 4 pages.

C45

Xiaojun Yang, C. Kachris, M. Katevenis: "Efficient Implementation for CIOQ Switches with Sequential Iterative Matching Algorithms", Proc. of the *IEEE Int. Conf. on Field-Programmable Technology (FPT 2010)*, doi: 10.1109/FPT.2010.5681453, Beijing, China, December 2010, pp. 433-436.

C44

C. Kachris, G. Nikiforos, S. Kavadias, V. Papaefstathiou, M. Katevenis: "Network Processing in Multi-core FPGAs with Integrated Cache-Network Interface", Proc. of the *IEEE Int. Conf. on Reconfigurable Computing and FPGAs (Reconfig 2010)*, Cancun, Mexico, December 2010.

C43

S. Kavadias, M. Katevenis, M. Zampetakis, D. Nikolopoulos: "On-chip Communication and Synchronization Mechanisms with Cache-Integrated Network Interfaces", Proc. of the *7th ACM Int. Conf. on Computing Frontiers (CF 2010)*, Bertinoro, Italy, 17-19 May 2010, pp. 217-226, doi.acm.org/10.1145/1787275.1787328

C42

G. Passas, M. Katevenis, D. Pnevmatikatos: "A 128x128x24Gb/s Crossbar, Interconnecting 128 Tiles in a Single Hop, and Occupying 6% of their Area", Proc. of the *4th ACM/IEEE Int. Symposium on Networks-on-Chips (NOCS 2010)*, Grenoble, France, 3-6 May 2010, pp. 87-95; IEEE Computer Society ISBN 978-0-7695-4049-8.

C41

G. Kalokerinos, V. Papaefstathiou, G. Nikiforos, S. Kavadias, M. Katevenis, D. Pnevmatikatos, Xiaojun Yang: "FPGA Implementation of a Configurable Cache/Scratchpad Memory with Virtualized User-Level RDMA Capability", Proc. of the *IEEE Int. Conf. on Embedded Computer Systems: Architectures, Modeling and Simulation (IC-SAMOS 2009)*, Samos, Greece, 20-23 July 2009, ISBN 978-1-4244-4501-1, pp. 149-156.

C40

V. Papaefstathiou, D. Pnevmatikatos, M. Marazakis, G. Kalokairinos, A. Ioannou, M. Papamichael, S. Kavadias, G. Mihelogiannakis, M. Katevenis: "Prototyping Efficient Interprocessor Communication Mechanisms", Proc. of the *IEEE Int. Conf. on Embedded Computer Systems: Architectures, Modeling and Simulation (IC-SAMOS 2007)*, Samos, Greece, 16-19 July 2007, pp. 26-33.

C39

N. Chrysos, M. Katevenis: "Crossbars with Minimally-Sized Crosspoint Buffers", Proc. of the

- IEEE Int. Conf. on High Performance Switching and Routing*, (**HPSR 2007**), Brooklyn, NY, USA, 30 May - 1 June 2007.
- C38** G. Passas, M. Katevenis: "Asynchronous Operation of Bufferless Crossbars", Proc. of the *IEEE Int. Conf. on High Performance Switching and Routing*, (**HPSR 2007**), Brooklyn, NY, USA, 30 May - 1 June 2007, ISBN 1-4244-1206-4, paper ID 1569017531.pdf.
- C37** G. Michelogiannakis, D. Pnevmatikatos, M. Katevenis: "Approaching Ideal NoC Latency with Pre-Configured Routes", Proc. of the *1st ACM/IEEE Int. Symposium on Networks-on-Chips* (**NOCS 2007**), Princeton, NJ, USA, 7-9 May 2007, pp. 153-162.
- C36** M. Katevenis, G. Passas: "Packet Mode Scheduling in Buffered Crossbar (CICQ) Switches", Proc. of the IEEE Workshop - later called *IEEE Int. Conf. on High Performance Switching and Routing*, (**HPSR 2006**), Poznan, Poland, 7-9 June 2006, pp. 105-112, ISBN 0-7803-9570-0.
- C35** N. Chrysos, M. Katevenis: "Preventing Buffer-Credit Accumulations in Switches with Shared Small Output Queues", Proc. of the IEEE Workshop - later called *IEEE Int. Conf. on High Performance Switching and Routing*, (**HPSR 2006**), Poznan, Poland, 7-9 June 2006, pp. 409-416, ISBN 0-7803-9570-0.
- C34** N. Chrysos, M. Katevenis: "Scheduling in Non-Blocking Buffered Three-Stage Switching Fabrics", Proc. of the IEEE **Infocom 2006** Conference, Barcelona, Spain, 23-29 Apr. 2006, 13 pages, CDROM paper ID 13_01.
- C33** N. Chrysos, M. Katevenis: "Scheduling in Switches with Small Internal Buffers", Proc. of the IEEE **Globecom 2005** Conference, St. Louis, MO, USA, 28 Nov. - 2 Dec. 2005, 6 pages, CDROM paper ID gc21_3.
- C32** M. Katevenis, G. Passas: "Variable-Size Multipacket Segments in Buffered Crossbar (CICQ) Architectures", Proc. of the *IEEE Int. Conf. on Communications* (**ICC 2005**), Seoul, Korea, 16-20 May 2005, CR-ROM paper ID "09GC08-4", 6 pages.
- C31** N. Chrysos, M. Katevenis: "Multiple Priorities in a Two-Lane Buffered Crossbar", Proc. of the IEEE **Globecom 2004** Conference, Dallas, TX, USA, 29 Nov. - 4 Dec. 2004, CR-ROM paper ID "GE15-3", 7 pages.
- C30** M. Katevenis, G. Passas, D. Simos, I. Papaefstathiou, N. Chrysos: "Variable Packet Size Buffered Crossbar (CICQ) Switches", Proc. of the *IEEE Int. Conf. on Communications* (**ICC 2004**), Paris, France, June 2004, vol. 2, pp. 1090-1096.
- C29** N. Chrysos, M. Katevenis: "Weighted Fairness in Buffered Crossbar Scheduling", Proc. of the IEEE Workshop - later called *IEEE Int. Conf. on High Performance Switching and Routing*, (**HPSR 2003**), Torino, Italy, June 2003, pp. 17-22;
- C28** G. Sapountzis, M. Katevenis: "Benes Switching Fabrics with O(N)-Complexity Internal Backpressure", Proc. of the IEEE Workshop - later called *IEEE Int. Conf. on High Performance Switching and Routing*, (**HPSR 2003**), Torino, Italy, June 2003, pp. 11-16.
- C27** A. Ioannou, M. Katevenis: "Pipelined Heap (Priority Queue) Management for Advanced Scheduling in High Speed Networks", Proc. of the *IEEE Int. Conf. on Communications* (**ICC 2001**), Helsinki, Finland, June 2001, pp. 2043-2047.
- C26** A. Nikologiannis, M. Katevenis: "Efficient Per-Flow Queueing in DRAM at OC-192 Line Rate using Out-of-Order Execution Techniques", Proc. of the *IEEE Int. Conf. on Communications* (**ICC 2001**), Helsinki, Finland, June 2001, pp. 2048-2052.
- C25** E. Markatos, M. Katevenis, D. Pnevmatikatos, M. Flouris: "Secondary Storage Management

for Web Proxies", *Proc. 2nd USENIX Symposium on Internet Technologies and Systems (USITS 1999)*, Boulder, CO USA, Oct. 1999, pp. 93-104.

- C24** G. Kornaros, D. Pnevmatikatos, P. Vatsolaki, G. Kalokerinos, C. Xanthaki, D. Mavroidis, D. Serpanos, M. Katevenis: "Implementation of ATLAS I: a Single-Chip ATM Switch with Backpressure", *Proc. of the IEEE Hot Interconnects 6 Symposium (HotI 1998)*, Stanford, California, USA, 13-15 August 1998, pp. 85-96.
- C23** M. Katevenis, D. Serpanos, E. Spyridakis: "Credit-Flow-Controlled ATM for MP Interconnection: the ATLAS I Single-Chip ATM Switch", *Proc. of the 4th IEEE Int. Symp. on High-Performance Computer Architecture (HPCA 1998)*, Las Vegas, NV USA, Feb. 1998, IEEE Computer Soc. Press, ISBN 0-8186-8323-6, pp. 47-56.
- C22** E. Markatos, M. Katevenis, P. Vatsolaki: "The Remote Enqueue Operation on Networks of Workstations", *Proceedings of the Workshop on Communication and Architectural Support for Network-Based Parallel Computing (CANPC 1998)*, Las Vegas, NV USA, 31 Jan. 1998, Lecture Notes in Computer Science 1362, Springer-Verlag, pp. 1-14.
- C21** M. Katevenis, D. Serpanos, E. Spyridakis: "Switching Fabrics with Internal Backpressure using the ATLAS I Single-Chip ATM Switch", *Proc. of the IEEE GLOBECOM 1997 Conference*, Phoenix, AZ USA, Nov. 1997, pp. 242-246.
- C20** M. Katevenis, D. Serpanos, E. Markatos: "Multi-Queue Management and Scheduling for Improved QoS in Communication Networks", *Proc. of the European Multimedia Microprocessor Systems and Electronic Commerce Conference (EMMSEC 1997)*, Florence, Italy, Nov. 1997, pp. 906-913.
- C19** G. Kornaros, C. Kozyrakis, P. Vatsolaki, M. Katevenis: "Pipelined Multi-Queue Management in a VLSI ATM Switch Chip with Credit-Based Flow Control", *Proc. of the 17th Conf. on Advanced Research in VLSI (ARVLSI 1997)*, Univ. of Michigan at Ann Arbor, MI USA, Sept. 1997, IEEE Computer Soc. Press, ISBN 0-8186-7913-1, pp. 127-144.
- C18** M. Katevenis: "Buffer Requirements of Credit-Based Flow Control when a Minimum Draining Rate is Guaranteed", *Proc. of the 4th IEEE Workshop on Architecture and Implementation of High Perf. Commun. Subsystems (HPCS 1997)*, Chalkidiki, Greece, June 1997.
- C17** D. Serpanos, M. Katevenis, E. Spyridakis: "ATLAS I: Building Block for ATM Networks with Credit-Based Flow Control", *Proc. of the 4th IEEE Workshop on Architecture and Implementation of High Perf. Commun. Subsystems (HPCS 1997)*, Chalkidiki, Greece, June 1997.
- C16** E. Markatos, M. Katevenis: "User-Level DMA without Operating System Kernel Modification", *Proc. of the 3rd IEEE Int. Symp. on High-Performance Computer Architecture (HPCA 1997)*, San Antonio, TX USA, Feb. 1997, pp. 322-331.
- C15** M. Katevenis, P. Vatsolaki, D. Serpanos, E. Markatos: "ATLAS I: A Single-Chip ATM Switch for NOWs", *Proc. of the Workshop on Communication and Architectural Support for Network-Based Parallel Computing (CANPC 1997)*, San Antonio, TX USA, Feb. 1997, Lecture Notes in Computer Science 1199, Springer-Verlag, pp.88-101.
- C14** M. Katevenis, P. Vatsolaki: "ATLAS I: A Single-Chip ATM Switch with HIC Links and Multi-Lane Back-Pressure", *Proc. of the 6th Annual OMI Conference: Embedded Microprocessor Systems, (EMSYS 1996)*, Berlin, Germany, Sep. 1996, IOS Press, ISBN 90-5199-300-5, pp. 126-136.
- C13** M. Katevenis, D. Serpanos, P. Vatsolaki: "ATLAS I: A General-Purpose, Single-Chip ATM Switch with Credit-Based Flow Control", *Proc. of the IEEE Hot Interconnects IV Symposium*

- (**HotI 1996**), Stanford Univ., CA, USA, Aug. 1996, pp. 63-73.
- C12** E. Markatos, M. Katevenis: ``Telegraphos: High-Performance Networking for Parallel Processing on Workstation Clusters'', Proc. of the *2nd IEEE Int. Symp. on High-Performance Computer Architecture (HPCA 1996)*, San Jose, CA USA, February 1996, pp.144-153.
- C11** M. Katevenis, P. Vatsolaki, A. Efthymiou: ``Pipelined Memory Shared Buffer for VLSI Switches'', Proc. of the *ACM SIGCOMM '95 Conference (SIGCOMM 1995)*, Cambridge, MA USA, 30 August - 1 Sep. 1995, pp. 39-48.
- C10** M. Katevenis, P. Vatsolaki, A. Efthymiou, M. Stratakis: ``VC-level Flow Control and Shared Buffering in the Telegraphos Switch'', Proc. of the *IEEE Hot Interconnects III Symposium (HotI 1995)*, Stanford Univ., CA, USA, Aug. 1995.
- C9** M. Katevenis, N. Tzartzanis: ``Reducing the Branch Penalty by Rearranging Instructions in a Double-Width Memory'', Proceedings of the *4th Int. Conf. on Architectural Support for Progr. Languages and Oper. Systems (ASPLOS 1991)*, Santa Clara, California, April 1991, pp. 15-27.
- C8** A. Vladimirescu, D. Weiss, M. Katevenis, Z. Bronstein, A. Kfir, K. Danuwidjaja, K. Ng, N. Jain, S. Lass: ``A Vector Hardware Accelerator with Circuit Simulation Emphasis'', Proceedings, *24th ACM/IEEE Design Automation Conference (DAC 1987)*, June 1987, pp. 89-94.
- C7** M. Katevenis, M. Blatt: ``Switch Design for Soft-Configurable WSI Systems'', Proc. of the *Conference on Advanced Research in VLSI (ARVLSI 1985)*, Univ. of North Carolina, Chapel Hill, May 1985.
- C6** R. Sherburne, M. Katevenis, D. Patterson, C. Sequin: ``A 32-Bit NMOS Microprocessor with a Large Register File'', Proceedings, *31st IEEE Int. Solid-State Circuits Conference (ISSCC 1984)*, San Francisco, February 1984, THAM 12.1, pp. 168-169.
- C5** R. Sherburne, M. Katevenis, D. Patterson, C. Sequin: ``Local Memory in RISCs'', Proceedings, *IEEE Int. Conf. on Computer Design: VLSI in Computers (ICCD 1983)*, New York, Nov. 1983, pp. 149-152.
- C4** M. Katevenis, R. Sherburne, D. Patterson and C. Sequin: ``The RISC II Micro-Architecture'', Proceedings of the *IFIP TC10/WG10.5 Int. Conference on Very Large Scale Integration (VLSI 1983)*, Trondheim, Norway, 16-19 Aug. 1983, North Holland Pub. Co., pp.349-359.
- C3** R. Sherburne, M. Katevenis, D. Patterson, C. Sequin: ``Datapath Design for RISC'', Proceedings, *Conference on Advanced Research in VLSI (ARVLSI)*, (**ARVLSI 1982**), M.I.T., Jan. 1982, pp. 53-62.
- C2** [**Fitz81**] D. Fitzpatrick, J. Foderaro, M. Katevenis, H. Landman, D. Patterson, J. Peek, Z. Peshkess, C. Sequin, R. Sherburne, K. VanDyke: ``VLSI Implementations of a Reduced Instruction Set Computer'', Proceedings of the *VLSI Systems and Computations Conference* -- later called *Conference on Advanced Research in VLSI (ARVLSI 1981)*, Carnegie-Mellon Univ., October 1981, Computer Science Press, pp. 327-336. Also published in: *Computer Architecture News (ACM SIGARCH)*, Vol. 10, No. 1, March 1982, pp. 28-32.
- C1** M. Katevenis, A. Arvillias, C. Halkias: ``Implementation of the FFT algorithm using the M6800 microprocessor'', Proc. of the *IEEE Int. Symposium on Circuits and Systems, (ISCAS 1979)*, Tokyo Japan, July 1979, p. 973. An extended version appeared in *Technika Chronika (ME-EE-NE section)*, Technical Chamber of Greece, Athens, Apr. 1979, pp.9-16.

2.6 Other Workshop and Technical Report Publications:

[**ANCS 2010**] N. Chrysos, L. Chen, C. Minkenberg, C. Kachris, M. Katevenis: "End-to-end congestion management for non-blocking multi-stage switching fabrics", *Proc. 2010 ACM/IEEE Symp. on Architecture for Networking and Communications Systems (ANCS 2010)*, San Diego, CA USA, 25-26 October 2010, pp. 6-7 (poster presentation).

[**CLUSTER 2010**] C. Kachris, G. Nikiforos, V. Papaefstathiou, S. Kavadias, M. Katevenis: "Low-latency Explicit Communication and Synchronization in Scalable Multi-core Clusters", Short paper and poster presented at the *IEEE Int. Conf. on Cluster Computing (CLUSTER 2010)*, Hersonissos, Crete, Greece, 20-24 September 2010.

[**SAMOS 2008**] M. Katevenis: "Towards Unified Mechanisms for Inter-Processor Communication", Keynote Presentation at the *IEEE Int. Conf. on Embedded Computer Systems: Architectures, Modeling and Simulation (IC-SAMOS VIII)*, Samos, Greece, 21-24 July 2008.

[**Stamatis 2007**] M. Katevenis: "Interprocessor Communication seen as Load-Store Instruction Generalization", Invited Paper in the Proc. of the *Stamatis Vassiliadis Symposium - The Future of Computing*, K. Bertels e.a. Editors, Delft, The Netherlands, 28 Sep. 2007, pp. 55-68.

[**EPY 1999**] G. Kornaros, D. Pnevmatikatos, D. Mavroidis, P. Vatsolaki, G. Kalokerinos, C. Xanthaki, G. Dimitriadis, D. Serpanos, M. Katevenis: "On Optimizing ATLAS I, a 10 Gbps ATM Switch", *Proc. 7th Panhellenic Informatics Conference*, Ioannina, Greece, August 1999. Also in *Advances in Informatics*, Fotiadis/Nikolopoulos Eds, World Scientific Publishing Co, ISBN 981-02-4192-5, pp. 164-177.

[**EPY 1995**] P. Vatsolaki, G. Kalokerinos, M. Stratakis, Ch. Xanthaki, M. Ligerakis, G. Kornaros, A. Dollas, G. Papadourakis, M. Katevenis: "The Implementation of Telegraphos: a High Speed Communication Architecture" (In Greek), *Proceedings of the 5th Panhellenic Informatics Conference*, Athens Greece, December 1995.

[**SCI 1995**] E. Markatos, M. Katevenis, G. Kalokerinos, D. Serpanos: "An Efficient Processor-Network Interface for Local Area Multiprocessors", *Proceedings of the 4th Int. Workshop on SCI-based High-Performance Low-Cost Computing*, SCiZZL, Crete Greece, 3 October 1995, pp. 23-32.

[**Seq. Consist. 1993**] J. Goodman, M. Katevenis: "A High-Speed Multiprocessor Network for Delivering Requests to Memory in Processor Time-Stamp Order" (method for achieving sequential consistency), *ESPRIT P6253 "SHIPS" Confidential Document*, summer 1993.

[**Mem. Barrier 1992**] P. Vatsolaki, M. Katevenis: "Implementation of the Memory Barrier in Multi-Stage Processor-Memory Networks", *ESPRIT P6253 "SHIPS" Confidential Working Document*, version 1.0, ICS-FORTH, Heraklion, Crete, 29 Dec. 1992.

(Innovative design for the method to implement the memory barrier operation in the processor to memory interconnection network of a parallel supercomputer).

[**Switch 1992**] M. Katevenis, G. Kalokerinos, P. Vatsolaki, E. Neonakis, M. Stratakis: "Internal Organizations of One-Cycle-Latency Crossbar Switch Chips", *ESPRIT P6253 "SHIPS" Confidential Working Document*, version 1.3, ICS-FORTH, Heraklion, Crete, 31 Dec. 1992.

(Design and evaluation --at the gate netlist level, verified by simulation in Verilog-- of three different organizations for the switch chip --in ECL gate-array technology, with 4 ns cycle time-- for processor to memory interconnection in a parallel supercomputer).

[**DEC Autonet 1988**] M. Katevenis: "The Autonet Switch: Architecture & Register-Transfer-Level Design", *Internal Memo, DEC Systems Research Center*, Palo Alto, CA, USA, 40 pages, Jan. 1988. (This was the preliminary switch design for "Autonet" -- a high-speed, self-configuring LAN using point-to-point links, precursor of DEC's "ATM GigaSwitch").

[**IEEE SCI 1987**] M. Katevenis: "Draft Ideas for a Backplane Superbus", *Memo to the IEEE "Superbus" (later "SCI") Committee*, California, USA, 17 pages, 10 December 1987.

(The IEEE "Superbus" Study Group was formed in 1987 in order to standardize a backplane bus in the 1 GByte/s throughput range. This was the first proposal to the group to base the new standard on a ring of point-to-point

connections rather than a bus. The Study Group later adopted this idea, renamed the project "Scalable Coherent Interface" (SCI), and developed ANSI/IEEE Standard 1596 (1992), which is based on rings of point-to-point connections).

[WSI 1986] M. Katevenis, M. Blatt: "Switch Design for Soft-Configurable WSI Systems", Proceedings of the IFIP WG 10.5 *Workshop on Wafer Scale Integration*, Grenoble, France, March 1986; Saucier, Trilhe, Eds, North Holland Co, ISBN 0-444-70103-6, pp. 255-270.

[RISC 1980] M. Katevenis: "A Proposal for the LSI Implementation of the RISC I CPU (using a 3-phase clock)", *U.C.Berkeley, CS Div., Internal Working Paper*, September 1980. (This internal working paper has served as the specification (block structure and timing) for the VLSI design of the RISC I NMOS single-chip 32-bit processor).

3. Research Grants

last updated: 20 April 2011

3.1 R&D Grants by the European Commission:

Research and development projects at [FORTH-ICS](#), funded by the European Commission following an evaluation of competing proposals, where Manolis Katevenis was the *Principal Investigator (PI)* at FORTH-ICS, or co-PI where noted as such:

- **ENCORE**: "ENabling technologies for a programmable many-CORE" (1/3/2010 - 28/2/2013; ICT FP7 STREP 248647), co-PI with Dimitris Nikolopoulos. FORTH-ICS budget: **533 k€**. Coordinating partner: Barcelona Supercomputing Center. Katevenis responsible for: architectural support and FPGA prototype for explicit communication in parallel processing on many-cores.
- **HiPEAC-2**: European Network of Excellence on "High Performance and Embedded Architecture and Compilation" (1/2/2008 - 31/1/2012; ICT FP7 NoE 217068). FORTH-ICS budget: **388 k€**. Coordinating partner: Ghent University, Belgium. FORTH-ICS task: Coordinator of the Interconnects Research Cluster and of the Task Force on Education and Training.
- **SARC**: "Scalable Computer Architecture" (1/1/2006 - 31/3/2010; FP6 FET IP 027648), co-PI with Angelos Bilas. FORTH-ICS budget: **1200 k€**. Coordinating partner: T.U. Delft, Netherlands. Katevenis responsible for: architectural support and FPGA prototype for low-latency, explicit interprocessor communication.
- **HiPEAC-1**: European Network of Excellence on "High Performance Embedded Architecture and Compilation" (1/9/2004 - 31/12/2008; ICT FP6 NoE 004408), co-PI with Angelos Bilas. FORTH-ICS budget: **246 k€**. Coordinating partner: UPC, Barcelona, Spain. FORTH-ICS task: research in computer architecture and in particular in interconnection networks, common computing equipment.
- **SISS**: "Scaleable Intelligent Video Server System" (1/1/2004 - 31/10/2006; ICT FP6 STREP), co-PI with Angelos Bilas. FORTH-ICS budget: **820 k€**. Coordinating partner: Xyratex Ltd, UK. Katevenis responsible for: novel architectural features for building scalable switches, switching fabrics, and low-latency network interfaces.
- **SPEAR-2**: 8-month feasibility study on a cost effective version of the SPARClet architecture dedicated to broadcast media embedded application (1/12/1997 - 31/7/1998). FORTH-ICS budget: **160 k€**. Coordinating partner: TSQUARE, France.
- **ARCHES**: "Application, Refinement, and Consolidation of HIC, Exploiting Standards" (1995 - 1997; ESPRIT IV). FORTH-ICS budget: **300 k€**. Coordinating partner: SGS Thomson, UK. FORTH-ICS task: participation in the architecture design of advanced network adapters.
- **ASICCOM**: "ATM Switch for Integrated Communication, Computation, and Monitoring" (1/9/1995 - 31/5/1999; ACTS 060). FORTH-ICS budget: **1400 k€**. Coordinating partner: Intracom

S.A., Peania, Greece. Technical Coordinator for the entire Project: M. Katevenis. FORTH-ICS task: architecture and chip design of *ATLAS I*, a 6-million-transistor single-chip 16x16 ATM switch with 32 thousand virtual channels of credit-based flow control; the chip was fabricated by ST Microelectronics.

- **AMUS** and **SHIPS**: "A Multiscalar Supercomputer" and "Supercomputer Highly Parallel System" (1/1/1991 - 31/5/1995; ESPRIT II 2716, ESPRIT III 6253). FORTH-ICS budget: **1800 k€**. Coordinating partner: Advanced Computer Research Institute (ACRI) S.A., Lyon, France. FORTH-ICS task: architectural studies for a parallel supercomputer; and the *Telegraphos* project: architecture, design, and implementation of prototypes for remote-write and remote-DMA based high-speed communication in parallel and distributed systems.
- **Hellenic-VLSI**: "Hellenic VLSI Design & Prototyping Environment" (1/1/1991 - 31/12/1993; ESPRIT II 5692 and STRIDE). FORTH-ICS budget: **210 k€**. FORTH-ICS task: designing a JPEG image-compression chip, and a control unit for a VHF amplifier.

3.2 R&D Grants from the Private Sector:

Research and development contracts to [FORTH-ICS](#) from private-sector companies, where Manolis Katevenis was the *Principal Investigator (PI)* at FORTH-ICS, or co-PI where noted as such:

- **Ellemedia** S.A., Athens, Greece (2003 - 2006), co-PI with Ioannis Papaefstathiou; FORTH-ICS budget: **160 k€**. FORTH-ICS task: Subsystem design and coding for ASIC and FPGA systems - MEDIAGATE, NPMAD, WEBSOC.
- **INACCESS** S.A., Athens, Greece (2002 - 2003), co-PI with Ioannis Papaefstathiou; FORTH-ICS budget: **45 k€**. FORTH-ICS task: DES and MMU subsystem design for ASIC's.
- **ISD** S.A., Athens, Greece (2000 - 2003); FORTH-ICS budget: **47 k€**. FORTH-ICS task: subsystem design for ASIC- and PCB-based digital systems.
- **Intracom** S.A., Athens, Greece (1998 - 1999); FORTH-ICS budget: **50 k€**. FORTH-ICS task: interfacing the ATLAS I switch chip (from the ASICCOM project) to a standard ATM network with OC-12 links (FASMA, MEMAS).
- **NISHAN** Systems Inc, San Jose, California USA (1999 - 2001); FORTH-ICS budget: **150 k€**. FORTH-ICS task: Consulting to Nishan Systems Inc. on Packet Switch Architectures and Chip Design for Storage Area Networks

3.3 R&D Grants by the Greek Government:

Research and development projects at [FORTH-ICS](#) funded by the Greek Government following an evaluation of competing proposals, where Manolis Katevenis was the *Principal Investigator (PI)* at FORTH-ICS:

- **PLATON** (2000 - 2001; PENED): FORTH-ICS budget: **65 k€**.
- **DIPOLO**: packet router implementation, at the PCB and embedded processor level, with advanced QoS features (1999 - 2001; EPET II); FORTH-ICS budget: **175 k€**.
- **EPET-Microelectronics**: "Development of Industrial Microelectronics products" (1/7/1995 - 31/12/1997; EPET II 476). FORTH-ICS budget: **40 k€**.
- **MOP-CAD**: "Mediterranean Integrated Program on Computer Aided Design" (1987 - 1992). FORTH-ICS budget: **400 k€**. FORTH-ICS task: CAD tools for various engineering disciplines.

3.4 Host Scientist for New Researchers with Marie-Curie Grants:

Manolis Katevenis was the *Host Scientist* for new researchers that came to [FORTH-ICS](#) funded by the following Marie-Curie European Commission Mobility Grants:

- **I-Cores**: "I-cores - Hypervisor-Based Synthesis of Custom Execution Environments on Multi-Core Systems" (1/12/2008 - 30/11/2012, int. reintegration grant). Principal Investigator: *Dimitris Nikolopoulos*; FORTH-ICS budget: **100 k€**.

- **ATHLOS** (2004-2008), int. reintegration grant. Principal Investigator: *Angelos Bilas*; FORTH-ICS budget: **80 k€**.
- **UNiSIX**: "Unifying High-speed Interconnects" (1/2/2005 - 31/1/2009, Marie-Curie Excellent Team). Principal Investigator: *Angelos Bilas*; FORTH-ICS budget: **1163 k€**.

4. Editorial and Conference Organization, PC Memberships

last updated: 20 April 2011

4.1 Editorial Board:

Manolis Katevenis is a member of the Editorial Board of the *Transactions on High-Performance and Embedded Architectures and Compilers (Transactions on HiPEAC)* - <http://www.hipeac.net/journal>

4.2 General Co-Chair:

Manolis Katevenis and Margaret Martonosi were General Co-Chairs for the *6th International Conference on High-Performance and Embedded Architectures and Compilers - HiPEAC'11*, Heraklion, Crete, Greece, 24-26 January 2011; <http://www.hipeac.net/hipeac2011>

4.3 Technical Program Committee (PC) Co-Chair:

Manolis Katevenis and Rajiv Gupta were Program Co-Chairs for the *3rd International Conference on High Performance Embedded Architectures and Compilers - HiPEAC 2008*, Goteborg, Sweden, 27-29 January 2008; <http://www.hipeac.net/hipeac2008>

4.4 Technical Program Committee (PC) Member:

Manolis Katevenis is or has been a Member of the Technical Program Committees for the following Conferences:

- **HiPC 2011** (18th Annual IEEE Int. Conf. on High Performance Computing), Bengaluru (Bangalore), India, 18-21 Dec. 2011; <http://www.hipc.org/hipc2011/>
- **SAMOS 2011** (IEEE Int. Conf. on Embedded Computer Systems: Architectures, Modeling and Simulation): Samos, Greece, 18-21 July 2011; http://samos.et.tudelft.nl/samos_xi/html/
- **Cluster 2010** (IEEE Int. Conf. on Cluster Computing 2010): Heraklion, Crete, Greece, 20-24 Sep. 2010; <http://www.cluster2010.org>
- **SAMOS 2010** (IEEE Int. Conf. on Embedded Computer Systems: Architectures, Modeling and Simulation): Samos, Greece, 20-23 July 2010; http://samos.et.tudelft.nl/samos_x
- **NOCS 2010** (4th ACM/IEEE Int. Symp. on Networks-on-Chip): Grenoble, France, 3-6 May 2010; <http://www.minatec.org/nocs2010/>
- **ANCS 2009** (5th ACM/IEEE Symp. on Architectures for Networking and Communications Systems): Princeton, NJ, USA, 19-20 Oct. 2009; <http://www.ancsconf.org>
- **ICPP 2009** (8th Int. Conf. on Parallel Processing): Vienna, Austria, 22-25 Sep. 2009; <http://www.cse.ohio-state.edu/~icpp2009/>
- **SAMOS 2009** (International Workshop on Systems, Architectures, Modeling, and Simulation - SAMOS Workshop): Samos, Greece, 20-23 July 2009; http://samos.et.tudelft.nl/samos_ix
- **NOCS 2009** (3rd ACM/IEEE Int. Symp. on Networks-on-Chip): San Diego, CA, USA, 10-13 May 2009; <http://circuit.ucsd.edu/~nocs2009/>
- **ARCS'09** (22nd Int. Conf. on Architecture of Computing Systems): T.U.Delft, Netherlands, 10-13 Mar. 2009; <http://www.ida.ing.tu-bs.de/arcs09/>
- **ANCS 2008** (4th ACM/IEEE Symp. on Architectures for Networking and Communications Systems): San Jose, CA, USA, 6-7 Nov. 2008; <http://www.ancsconf.org>
- **dasCMP 2008** (Workshop on Design, Architecture and Simulation of Chip Multi-Processors, held in conjunction with the 41st Annual International Symposium on Microarchitecture): Lake Como Italy, 9 Nov. 2008; <http://passat.crhc.uiuc.edu/dasCMP>

- **HPSR 2008** (IEEE International Conference on High Performance Switching and Routing): Shanghai, China, 15-17 May 2008; <http://www.hpsr2008.odu.edu/>
- **SAMOS VIII** (International Workshop on Systems, Architectures, Modeling, and Simulation - SAMOS Workshop): Samos, Greece, 21-24 July 2008; http://samos.et.tudelft.nl/samos_viii
- **ANCS 2007** (3rd ACM/IEEE Symp. on Architectures for Networking and Communications Systems): Orlando, Florida, USA, 3-4 Dec. 2007; <http://www.ancsconf.org>
- **ICS'07** (21st ACM Int. Conf. on Supercomputing): Seattle WA, USA, June 2007; <http://www.ics-conference.org>
- **DATE 2007** (Design and Test in Europe): Nice, France, Apr. 2007.
- **IPDPS 2007** (21st IEEE Int. Parallel and Distributed Processing Symposium): Long Beach, CA, USA, 26-30 March 2007; <http://www.ipdps.org>
- **HiPEAC 2007** (Int. Conf. on High-Performance Embedded Architectures and Compilers): Ghent, Belgium, Jan. 2007.
- **DSD'2007** (Euromicro Conf. on Digital System Design).
- **ANCS 2006** (2nd ACM/IEEE Symp. on Architectures for Networking and Communications Systems): San Jose, CA, USA, Dec. 2006.
- **ICS'06** (20th ACM Int. Conf. on Supercomputing): Queensland, Australia, June 2006.
- **DATE 2006** (Design and Test in Europe): Munich, Germany, March 2006.
- **HiPEAC 2005** (Int. Conf. on High-Performance Embedded Architectures and Compilers): Barcelona, Spain, Nov. 2005.
- **HotI 2004** (IEEE Symposium on High Performance Interconnects): Stanford, California, Aug. 2004.
- **NP3** (Workshop on Network Processors & Applications, in conjunction with HPCA): Madrid, Spain, Feb. 2004.
- **CAC'04** (Workshop on Communication Architecture for Clusters, in conjunction with IPDPS): Santa Fe, New Mexico, USA, Apr. 2004.
- **CAC'03** (Workshop on Communication Architecture for Clusters, in conjunction with IPDPS): Nice, France, Apr. 2003.
- **ISHPC-V** (5th Intl. Symp. on High-Performance Computing): Tokyo, Japan, Oct. 2003.
- **ICS'01** (ACM Int. Conf. Supercomputing): Sorrento, Italy June, 2001.
- **ICS'00** (ACM Int. Conf. Supercomputing): Santa Fe, NM May 2000.
- **EURO-PAR 2000**: Global Chairman for "Routing and Communication in Interconnection Networks", Munich, Germany, Sep. 2000.
- **HPCS'97** (4th IEEE Workshop on the Architecture and Implementation of High Performance Communication Subsystems): Chalkidiki, Greece, June 1997.
- **EURO-PAR'95**: Stockholm, Sweden, August 1995.
- **ISCA-22** (ACM/IEEE Int. Symp. on Computer Architecture): Portofino, Italy, June 1995.
- **ISCA-20** (ACM/IEEE Int. Symp. on Computer Architecture): San Diego, CA, USA, May 1993.
- **ASPLOS IV** (ACM/IEEE Int. Conf. on Architectural Support for Programming Languages and Operating Systems): Santa Clara, CA, USA, April 1991.
- **ASPLOS III** (ACM/IEEE Int. Conf. on Architectural Support for Programming Languages and Operating Systems): Boston, MA, USA, April 1989.

4.5 Workshop Organization and Steering Committee Member:

- Manolis Katevenis organized the *1st HiPEAC Workshop on Interconnection Network Architectures: On-Chip, Multi-Chip (INA-OCMC 2007)*, Ghent, Belgium, 28 Jan. 2007, held in conjunction with the HiPEAC 2007 Int. Conf. on High Performance Embedded Architectures and Compilers; <http://www.hipeac.net/node/716>
- Katevenis was a member of the Program Committee of the *2nd INA-OCMC Workshop*, Goteborg, Sweden, 27 Jan. 2008, held in conjunction with the HiPEAC 2008 Conference.
- Katevenis was a member of the Steering Committee of the 3rd through 5th *INA-OCMC Workshop*, years 2009 through 2011, held in conjunction with the corresponding HiPEAC Conferences; <http://ina-ocmc.et.tudelft.nl>
- Katevenis was and is a member of the Steering Committee of the *International Conference on High Performance and Embedded Architectures and Compilers (HiPEAC)*, for the years 2009 and 2012, http://www.hipeac.net/HiPEAC_conferences

5. Invited Lectures and Conference Presentations

last updated: 20 April 2011

5.1 Invited Plenary Talks:

- [BMW 2010](#): "Replicate and Migrate Objects in the Runtime, not Cache Lines or Pages in Hardware" (Invited Plenary Lecture), *Barcelona Multicore Workshop 2010*, Barcelona, Spain, 21-22 Oct. 2010.
- [SAMOS 2010](#): "Critical Problems and Opportunities in the emerging Multi-Core Era" (Plenary Panel Member), *IEEE Int. Conf. on Embedded Computer Systems: Architectures, Modeling and Simulation*: Samos, Greece, 19-21 July 2010.
- [SAMOS 2008](#): "Towards Unified Mechanisms for Inter-Processor Communication" (Keynote Presentation), *IEEE Int. Conf. on Embedded Computer Systems: Architectures, Modeling and Simulation*: Samos, Greece, 21-24 July 2008.
- [Stamatis 2007](#): "Interprocessor Communication seen as Load-Store Instruction Generalization" (Invited Plenary Lecture), *Stamatis Vassiliadis Symposium - The Future of Computing*, Delft, The Netherlands, 28 Sep. 2007.
- [OCIN 2006](#): "Towards Light-Weight Intra-CMP Network Interfaces" (Invited Plenary Lecture), *Workshop on On- and Off-Chip Interconnection Networks for Multicore Systems*, Stanford, California, USA, 6-7 Dec. 2006.
- [ERCIM \(1993\)](#): "Parallel Computer Architecture: Shared Memory versus Message Passing" (Invited Lecture), Symposium of the European Research Consortium for Informatics and Mathematics (ERCIM), Rutherford Appleton Laboratory, UK, 10-12 November 1993.

5.2 Invited Lectures and Seminars:

- [U. Cyprus \(2009\)](#): "Towards Unified Mechanisms for Inter-Processor Communication" (Invited Lecture), Computer Science Dept., University of Cyprus, Nicosia, Cyprus, 30 January 2009.
- [ACACES 2007](#): "Queue and Flow Control Architectures for Interconnection Switches" (4-Lecture Invited Course), *3rd Int. Summer School on Advanced Computer Architecture and Compilation for Embedded Systems*, L'Aquila, Italy, 15-20 July 2007.
- [Stanford \(2006\)](#): "Intra-CMP Light-Weight Network Interfaces, and their FPGA Prototyping" (Seminar Talk), Electrical Eng. Dept., Stanford University, California, USA, 4 December 2006.
- [T.U. Delft \(2005\)](#): "Packet Switch Architecture and Buffered Crossbar Switches" (Seminar Talk), Electrical Eng. Dept., Delft University of Technology, The Netherlands, 10 May 2005.
- [U. of Athens \(2004\)](#): "Digital Systems Architecture - the global situation and the position of Europe and Greece" (Invited Lecture), Dept. of Informatics, University of Athens, Greece, 1 October 2004.
- [Zappeion \(2000\)](#): "Microelectronics and High-Speed Networks" (invited presentation to the wide public), Zappeion Exhibition and Congress Hall, Athens, Greece, May 2000.
- [Siemens \(1990\)](#): "Forthcoming Opportunities for VLSI Electronic System Design in the Science and technology Park of Crete" (Seminar Talk), Siemens, Germany, September 1990.
- [CERN \(1989\)](#): "The Design of the RISC II Processor at U.C.Berkeley" (Seminar Talk), CERN, Geneva, Switzerland, 25 January 1989.
- [EPY \(1988\)](#): "Modern VLSI Technology and RISC Architectures" (Seminar Talk), Informatics Professionals Union of Greece (EPY), Athens, Greece, November 1988.
- [Stanford \(1987\)](#): "Fast Switching and Fair Control of Congested Flow in Broad-Band Networks", Computer Systems Colloquium, Stanford University, California, USA, 2 December 1987.
- [NTUA \(1987\)](#): "Fast Switching and Fair Control of Congested Flow in Broad-Band Networks" (Seminar Talk), National Technical University of Athens (NTUA), Greece, June 1987.
- [Air Force \(1986\)](#): "Switching Circuit Design for Wafer-Scale Integration" (Invited Lecture), Greek Air Force Research Center, Athens, Greece, November 1986.
- [CERN \(1986\)](#): "Design of VLSI Circuits" and "Capabilities and Limitations of VLSI Circuits" (2-lecture course), and "Reduced Instruction Set Computer Architectures" (Invited Lecture), 1986 CERN School of Computing, Geneva, Switzerland, September 1986.

- **Darmstadt (1986)**: "Reduced Instruction Set Computer Architectures for VLSI", and "Switch Design for Soft-Configurable WSI Systems" (Invited Lectures), EIS-CAD-VLSI Summer School, Technische Hochschule Darmstadt, West Germany, June 1986.
- **CAVE (1986)**: "Experience with the CAD Tools while designing the RISC II Processor" (Invited Plenary Lecture), *CAD for VLSI in Europe Workshop (CAVE)*, Patras, Greece, May 1986.
- **FACE (1985)**: "RISC Architectures" and "Soft-Configurable Wafer-Scale Integration" (Invited Lectures), FACE Research Centre, Pomezia, Italy, May 1985.
- **MIT (1984)**: "Switch Design for Soft-Configurable Wafer-Scale Integrated Systems" (Invited Lecture), Lincoln Lab, Massachusetts Institute of Technology, MA USA, 18 December 1984.
- **UMASS (1984)**: "Fast-Operand-Access- and Reduced-Instruction-Set- Computer Architectures" (Seminar Talk), University of Massachusetts at Amherst, MA USA, December 1984.
- **Stanford CIS (1984)**: "RISCy Microcomputers and Risky Wafers" (Invited Lecture), Center for Integrated Systems, Stanford University, November 1984.
- **Stanford Forum (1984)**: "Balancing Complexity and Simplicity in VLSI Design" (Invited Lecture), Computer Forum, Stanford University, February 1984.
- **Stanford CSL (1984)**: "Reduced Instructions and Fast Operand Access for General Purpose Microprocessors" (Seminar Talk), Computer Systems Lab, Stanford University, February 1984.
- **Intel (1983)**: "Designing RISC II" (Invited Lecture), Intel, Santa Clara, California, USA, 19 December 1983.
- **RISC (1983)**: "RISC Architectures for VLSI", Interview Talk, given in March 1983 at: (i) Bell Laboratories, Murray Hill, NJ; (ii) IBM, T.J.Watson Research Center; (iii) Carnegie-Mellon University, Pittsburgh, PA; (iv) Columbia University, New York, NY; (v) Duke University, Durham, NC; (vi) University of Illinois, Urbana, IL; (vii) Massachusetts Institute of Technology, Cambridge, MA; (viii) University of Maryland, College Park, MD; (ix) New York University, New York, NY; (x) Princeton University, Princeton, NJ; (xi) University of California, Los Angeles, CA; (xii) University of North Carolina, Chapel Hill, NC; (xiii) University of Washington, Seattle, WA; and (xiv) University of Wisconsin, Madison, WI.
- **Stanford CSL (1982)**: "The RISC Architecture" (Seminar Talk), Computer Systems Lab, Stanford University, November 1982.

5.3 Presentations at Conferences and Workshops:

- **SAMOS 2009**: "FPGA Implementation of a Configurable Cache/Scratchpad Memory with Virtualized User-Level RDMA Capability", at the *IEEE Int. Conf. on Embedded Computer Systems: Architectures, Modeling and Simulation (IC-SAMOS IX)*: Samos, Greece, 20-23 July 2009.
- **Infocom (2006)**: "Scheduling in Non-Blocking Buffered Three-Stage Switching Fabrics", at the *IEEE Infocom 2006 Conference*, Barcelona, Spain, 23-29 Apr. 2006.
- **ICC (2004)**: "Variable Packet Size Buffered Crossbar (CICQ) Switches", at the *IEEE Int. Conf. on Communications (ICC 2004)*, Paris, France, June 2004.
- **HPSR (2003b)**: "Weighted Fairness in Buffered Crossbar Scheduling", at the *IEEE Workshop on High Performance Switching and Routing (HPSR 2003)*, Torino, Italy, June 2003.
- **HPSR (2003a)**: "Benes Switching Fabrics with O(N)-Complexity Internal Backpressure", at the *IEEE Workshop on High Performance Switching and Routing (HPSR 2003)*, Torino, Italy, June 2003.
- **ICC (2001b)**: "Efficient Per-Flow Queueing in DRAM at OC-192 Line Rate using Out-of-Order Execution Techniques", at the *IEEE Int. Conf. on Communications (ICC 2001)*, Helsinki, Finland, June 2001.
- **ICC (2001a)**: "Pipelined Heap (Priority Queue) Management for Advanced Scheduling in High Speed Networks", at the *IEEE Int. Conf. on Communications (ICC 2001)*, Helsinki, Finland, June 2001.
- **HotI (1998)**: "Implementation of ATLAS I: a Single-Chip ATM Switch with Backpressure", at the *IEEE Hot Interconnects 6 Symposium*, Stanford, California, USA, 13-15 August 1998.
- **HPCA (1998)**: "Credit-Flow-Controlled ATM for MP Interconnection: the ATLAS I Single-Chip ATM Switch" at the *4th IEEE Int. Symposium on High-Performance Computer Architecture*, Las Vegas, Nevada, Feb. 1998.
- **CANPC (1998)**: "The Remote Enqueue Operation on Networks of Workstations", at the *Workshop on Communication and Architectural Support for Network-Based Parallel Computing (CANPC)*, Las Vegas, Nevada, 31 Jan. 1998.
- **GLOBECOM (1997)**: "Switching Fabrics with Internal Backpressure using the ATLAS I Single-

Chip ATM Switch", at the *IEEE GLOBECOM'97 Conference*, Phoenix, AZ USA, Nov. 1997.

- **ARVLSI (1997)**: "Pipelined Multi-Queue Management in a VLSI ATM Switch Chip with Credit-Based Flow Control", at the *17th Conference on Advanced Research in VLSI (ARVLSI)*, Ann Arbor, Michigan, Sept. 1997.
- **HPCS (1997b)**: "Buffer Requirements of Credit-Based Flow Control when a Minimum Draining Rate is Guaranteed", at the *4th IEEE Workshop on Arch. & Impl. of High Perf. Commun. Subsystems (HPCS)*, Chalkidiki, Greece, June 1997.
- **HPCS (1997a)**: "ATLAS I: Building Block for ATM Networks with Credit-Based Flow Control", at the *4th IEEE Workshop on Arch. & Impl. of High Perf. Commun. Subsystems (HPCS)*, Chalkidiki, Greece, June 1997.
- **EMSYS (1996)**: "ATLAS I: A Single-Chip ATM Switch with HIC Links and Multi-Lane Back-Pressure", at the *6th Annual Conference on Embedded Microprocessor Systems (EMSYS)*, Berlin, Germany, Sep. 1996.
- **HotI (1996)**: "ATLAS I: A General-Purpose, Single-Chip ATM Switch with Credit-Based Flow Control", at the *IEEE Hot Interconnects IV Symposium*, Stanford Univ., CA, USA, Aug. 1996.
- **SCIzzL (1995)**: "An Efficient Processor-Network Interface for Local Area Multiprocessors", at the *4th Int. Workshop on SCI-based High-Performance Low-Cost Computing*, Crete Greece, 3 October 1995.
- **SIGCOMM (1995)**: "Pipelined Memory Shared Buffer for VLSI Switches", at the *ACM SIGCOMM '95 Conference*, Cambridge, MA USA, 30 August - 1 Sep. 1995.
- **HotI (1995)**: "VC-level Flow Control and Shared Buffering in the Telegraphos Switch", at the *IEEE Hot Interconnects III Symposium*, Stanford Univ., CA, USA, Aug. 1995.
- **ERCIM (1994)**: "Where should Research on Parallel Computer Architectures focus in the next few years?" (Invited Lecture), *European Research Consortium for Informatics and Mathematics (ERCIM) PPN Workshop*, Heraklion, Crete, Greece, June 1994.
- **ASPLOS (1991)**: "Reducing the Branch Penalty by Rearranging Instructions in a Double-Width Memory", at the *4th Int. Conf. on Architectural Support for Progr. Languages and Oper. Systems (ASPLOS)*, Santa Clara, California, April 1991.
- **WSI (1986)**: "Switch Design for Soft-Configurable WSI Systems", at the *Workshop on Wafer Scale Integration - IFIP WG 10.5*, Grenoble, France, March 1986.
- **ARVLSI (1985)**: "Switch Design for Soft-Configurable WSI Systems", at the *Conference on Advanced Research in VLSI (ARVLSI)*, Chapel Hill, North Carolina, May 1985.
- **VLSI (1983)**: "The RISC II Micro-Architecture", at the *Int. Conference on Very Large Scale Integration (VLSI '83)*, Trondheim, Norway, 16-19 Aug. 1983.
- **ARVLSI (1982)**: "Datapath Design for RISC", at the *Conference on Advanced Research in VLSI (ARVLSI)*, Cambridge, Massachusetts, January 1982.

6. Graduate Students and Alumni

last updated: 20 April 2011

6.1 Current PhD Students:

- **Giorgos Passas**
- [Vassilis Papaefstathiou](#)

6.2 Graduated PhD Students:

- [Stamatis Kavadias](#) (PhD. December 2010; Thesis: "Direct Communication and Synchronization Mechanisms in Chip Multiprocessors")
- **Nikos Chrysos** (PhD. December 2006; Thesis: "Request-Grant Scheduling for Congestion Elimination in Multistage Networks"; first job: IBM Zurich Research Lab)

6.3 Distinguished Alumni:

- [Andreas Moshovos](#), Associate Professor, University of Toronto, recipient of the 2010 ACM

SIGARCH Maurice Wilkes award (PhD. 1998 U.Wisconsin-Madison) (MSc. 1992 U.Crete advised by M. Katevenis - thesis: "Implementing Non-Numerical Algorithms on an Access Decoupled Architecture that supports Software Pipelining")

- [Christos Kozyrakis](#), Associate Professor, Stanford University (PhD. 2002 U.C. Berkeley) (BSc. 1996 U.Crete advised by M. Katevenis - thesis: "The Architecture, Operation, and Design of the Queue Management Block in the ATLAS I ATM Switch")
- [Stefanos Sidiropoulos](#), VP, Netlogic Microsystems, ex-founder, CEO, and CTO of Aeluros Inc. (PhD. 1997 Stanford Univ.) (MSc. 1991 U.Crete advised by M. Katevenis - thesis: "Weighted Round-Robin Cell Multiplexing in a General-Purpose ATM Switch Chip")
- [Nestoras Tzartzanis](#), Research Scientist, Apple (PhD. 1998 USC) (MSc. 1991 U.Crete advised by M. Katevenis - thesis: "Reducing the Branch Penalty by Rearranging Instructions in a Double-Width Memory")
- [Dionisios Pnevmatikatos](#), Professor, Technical University of Crete (PhD. 1995 and MSc 1991 U.Wisconsin-Madison) (BSc. 1989 U.Crete, worked with M. Katevenis on a TTL prototype using a backpressured ring to replace a tristate bus)
- [Ioannis Papaefstathiou](#), Assistant Professor, Technical University of Crete (PhD. 2000 U. Cambridge, UK) (MSc 1997 Harvard U.) (BSc. 1996 U.Crete advised by M. Katevenis - thesis: "A behavioral model of the ATLAS I switch for providing inputs and for checking the outputs of the Queue Management Block")
- [Aristides Efthymiou](#), Lecturer (Assistant Professor), University of Edinburgh, UK (PhD. 2002 U. Manchester) (MSc. 1995 U.Crete advised by M. Katevenis - thesis: "Design, Implementation, and Testing of a 25 Gb/s Pipelined Memory Switch Buffer in Full-Custom CMOS")
- [Nikos Hardavellas](#), Assistant Professor, Northwestern University, Evanston, IL USA (PhD. 2009 and MSc. 2006 CMU) (BSc. 1995 U.Crete advised by M. Katevenis)

6.4 Graduated MSc Students:

- 2011: **Dimitris Tsaliagos**
- 2009: **Georgios Nikiforos**
- 2007: [Michael Papamichael](#), [Georgios Michelogiannakis](#)
- 2006: **Giorgos Passas**, [Evangelos Vlachos](#)
- 2004: **Dimitris Simos**
- 2002: **Dimitris Capsalis**, **Nikos Chrysos**, **Costas Harteros**, **Spyros Lyberis**, **Dimitris Meidanis**, **Giorgos Sapountzis**
- 2001: **Christos Lolas**, **George Papadakis**
- 2000: **Aggelos Ioannou**, **Aris Nikologiannis**
- 1998: **Georgios Glykopoulos**
- 1997: **Georgios Kornaros**
- 1996: **Manolis Spyridakis**
- 1995: [Aristides Efthymiou](#)
- 1994: **Giorgos Dimitriadis**, **Maria Karavassili**, **Chara Xanthaki**
- 1993: **Iasson Farsaris**, **Nikos Karydis**
- 1992: **Christos Georgis**, **Panagiotis Kalogerakis**, **Achileas Mantzios**, [Andreas Moshovos](#), **Tassos Sorilos**, **Peny Vatsolaki**
- 1991: [Stefanos Sidiropoulos](#), **Nestoras Tzartzanis**
- 1990: **Vaggelis Halkiadakis**

6.5 Member (other than Chair) of PhD Thesis Committees:

- **German Rodriguez**, UPC, Barcelona, Spain (2011)
- **Iakovos Mavroidis**, **Evrpidis Sotiriadis**, Technical Univ. of Crete, Chania, Greece (2011)
- **Miquel Moreto**, UPC, Barcelona, Spain (2010)
- **Lotfi Mhamdi**, T.U. Delft, Netherlands (2007)
- **Pedro Javier Garcia**, UCLM, Spain (2006)

7. Courses taught, New Courses introduced

last updated: 20 April 2011

7.1 Courses Taught:

- [CS-534 - Packet Switch Architecture](#): Graduate course, CS Dept., Univ. of Crete (taught 12 times: Sp'96, Sp'98, and Sp'00 with Stamoulis; F'01, Sp'03, Sp'04, Sp'05, Sp'06, Sp'07, Sp'08, Sp'09, Sp'11).
- [CS-120 - Digital Design](#): 1st year undergraduate core course, CS Dept., Univ. of Crete (taught 10 times: F'85, F'02, F'03, F'04, F'05, F'06, F'07, F'08, F'09, F'10).
- [CS-121 - Electric Circuits](#): Undergraduate introductory elective course, CS Dept., Univ. of Crete (taught twice: Sp'10, Sp'11).
- [CS-225 - Computer Organization](#): 2nd year undergraduate core course, CS Dept., Univ. of Crete (taught 14 times: Sp'86, Sp'87, F'93, Sp'96; Sp'99 with Serpanos; Sp'01, Sp'02; Sp'03 with Y. Papaefstathiou; Sp'04 through Sp'08 with Bilas; Sp'09 with Nikolopoulos).
- **CS-425 - Computer Architecture**: Senior undergraduate / introductory graduate elective course, CS Dept., Univ. of Crete (taught 13 times: Sp'86, F'88, F'89, Sp'91, F'92, Sp'94, F'96, F'99, F'00, F'03 with Bilas and Y. Papaefstathiou, F'04 with Bilas and J. Mavroidis, F'05 and F'06 with Bilas and Karlsson)
- **CS-625 - Advanced Computer Architecture**: Graduate course, CS Dept., Univ. of Crete (taught 3 times: Sp'90, Sp'92, Sp'01)
- **CS-422 - Introduction to VLSI Systems**: Senior undergraduate / introductory graduate elective course, CS Dept., Univ. of Crete (taught 9 times: Sp'87, Sp'89, Sp'91, Sp'93, Sp'95, Sp'98, F'99, F'00, F'02 with Sotiriou)
- **CS-523 - Computer Aided Design of Digital Systems**: Graduate course, CS Dept., Univ. of Crete (taught twice: F'85, Sp'01)
- **CS-520 - Semi-Custom ASIC Design**: Graduate course, CS Dept., Univ. of Crete (taught with Papadourakis in Sp'92)
- **CS-321 - Digital MOS Electronic Circuits**: Undergraduate elective course, CS Dept., Univ. of Crete (taught 5 times, with Traganitis: F'88, F'89, F'90, F'92, F'94)
- **CS-320 - Microprocessors and Peripherals**: Undergraduate elective course, CS Dept., Univ. of Crete (taught F'86)
- **CS-345 - Operating Systems**: Undergraduate core course, CS Dept., Univ. of Crete (taught twice: Sp'88, Sp'89)
- **CS-240 - Data Structures**: Undergraduate core course, CS Dept., Univ. of Crete (taught F'90)
- **CS-100 - Introduction to Computer Science**: Undergraduate core course, CS Dept., Univ. of Crete (taught twice: F'95, F'98)
- **EE-271 - Introduction to VLSI Systems**: Senior undergraduate / introductory graduate course, Electrical Eng. Dept., *Stanford University* (taught twice: Winter'85, F'87)
- **EE-272A - Design Projects in VLSI Systems**: Senior undergraduate / introductory graduate course, Electrical Eng. Dept., *Stanford University* (taught Winter'84)
- **CS-311 - Computer Systems Architecture**: Graduate course, Computer Sci. Dept., *Stanford University* (taught twice: Sp'84; F'84 with F. Baskett)
- [ACACES 2007](#): "Queue and Flow Control Architectures for Interconnection Switches" (4-Lecture Invited Course), *3rd Int. Summer School on Advanced Computer Architecture and Compilation for Embedded Systems*, L'Aquila, Italy, 15-20 July 2007.

7.2 New Courses Introduced:

- [CS-534 - Packet Switch Architecture](#) (graduate course, CS Dept., Univ. of Crete): course content has been innovative world-wide to some extent, partly based on own research results.
- [CS-120 - Digital Design](#) (1st year undergraduate core course, CS Dept., Univ. of Crete): course content developed for the specific teaching requirements, including our custom Lab Equipment ([photo](#)) and a novel datapath board of ours for a very simple computer ([photo](#)).
- [CS-225 - Computer Organization](#) (2nd year undergraduate core course, CS Dept., Univ. of Crete):

course content developed for the specific teaching requirements, including the specific set of exercises and simulation mini-project.

- At the University of Crete, CS Dept., Katevenis was the first to teach the following courses, having thus contributed to adapting their content to the specific environment: **CS-425**, **CS-625**, **CS-422**, **CS-423**, **CS-321**, **CS-320**,
- At Stanford University, in 1984-85, Katevenis reorganized the laboratory and the exercises of the **EE-271/272A (VLSI Design)** courses, using -for the first time- colour workstations and graphics editors.