Iakovos Mavroidis

PERSONAL

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Date of birth: 28 January 1978

Military service: 9/02 – 1/04

EDUCATION

- **Ph.D. Degree in Electronic and Computer Engineering, Technical University of Crete** (April 2011)
  Thesis Title: "Novel Techniques for Hardware/Software Partitioning and Emulation"
  Research Advisor: Prof. Ioannis Papaefstathiou

- **M.Sc. Degree in Computer Science, University of California at Berkeley** (July 2001)
  Thesis Title: "A Low Power 200MHz Multiported Register File for the Vector-IRAM chip"
  Research Advisors: Prof. David Patterson and Jan Rabaey
  GPA: 3.93 (out of 4)

- **B.Sc. Degree in Computer Science, University of Crete, Greece** (July 1999)
  GPA: 9.29 (out of 10)

TEACHING EXPERIENCE

- 2011 – now: **Visiting Instructor (Π.Δ. 407), Department of Electrical Engineer, Technical University of Crete.** Class:
  - Computer Architecture

- Spring 2012: **Instructor** of the "CMOS Technology for Computer Architects" (http://www.ics.forth.gr/~jacob/cmos4arch/) joint graduate course, offered to University of Crete, Chalmers, and Universitat Politècnica de Catalunya.

- 3/08 – 8/08: **Visiting Instructor (Π.Δ. 407), Department of Electrical Engineer, Technical University of Crete.** Class:
  - Computer Architecture

- 9/04 – 8/06, Fall 2012: **Visiting Instructor (Π.Δ. 407), Department of Computer Science, University of Crete.** Classes:
  - CS-422 Introduction to VLSI Systems
  - CS-425 Computer Architecture

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  - CS-220 Digital Circuit Lab
  - CS-523 Digital Systems CAD Lab

- 10/07-2/12: **Laboratory Instructor, Applied Informatics and Multimedia Department, Technological Educational Institute of Crete**, Classes:
  - Computer Architecture
  - Digital Design

WORK EXPERIENCE

- 8/07 – 6/10: **Assistant Manager, Integrated Systems Group, VTRIP (**www.vtrip.net**), Heraklion, Greece.**
  Worked on the development of the Solo Gateway product. Solo provides a unified communication and server solution (email, web, file, LDAP servers, analog & VoIP PBX, fax server, antivirus/antispam, VPN, automated backups & updates, collaboration tools, etc.) offering a flexible infrastructure for small and medium enterprises. Used Python and PHP under CentOS linux.

- 3/06 – 3/07: **Senior Digital Systems Design Engineer**, **Intracom Telecom (**www.intracom.com**), Athens, Greece.** Worked on the design and testing of two network cards. Main projects:

  - **Lead Designer** of a SONET terminal card for the RPR-STM-16 system, as part of the IBAS program. The card supports six Gigabit Ethernet ports, two optical STM-16 ports, four DDR chips, two Xilinx FPGAs and a CAM. The functionality of the card has been tested and verified.

  - **Lead Designer** of a TDM card that supports three TDM ports and two Gigabit Ethernet ports.

- 2/04 – 12/05: **Senior Digital Systems Design & Verification Engineer**, **Ellemedia Technologies, Heraklion, Greece**. Work comprised activities such as project design, implementation and verification, writing of technical documents and publications, and submitting of research projects to the EU and GSRT. Main projects:

  - **Lead Designer** of the NPMADE project. Designed and built on a Virtex-II Pro Xilinx FPGA the main functionality of the NPMADE network processor, a SoC design that incorporates 4 small DLX processors, a RISC processor and three Gigabit ports in order to manipulate, modify and route Ethernet traffic. Tested on the DiniGroup board prototype the functionality of the system that successfully manipulates and routes real IP traffic between NT workstations.

  - **Technical Lead** and author of the VPlanet project, a novel hardware accelerator/emulator system, which has been accepted and funded by the GSRT.

- 6/01 – 8/02: **Senior Digital Systems Design & Verification Engineer**, **MIPS Technologies** (www.mips.com), **Mountain View, CA, USA**. Worked on the design and verification of two RISC processors. Main projects:

  - **Designer** for the R20K microprocessor. Responsible for the Load Store Unit (LSU) and the Memory Management Unit (MMU) of a dual-issue high performance microprocessor. Designed, implemented and debugged various parts of the LSU, MMU, IFU and BIU units of the chip in Verilog, such as the *LRF* memory access algorithm of the cache, *BIST* algorithm for cache testing, the *External Request FSM* for multiprocessor communication, and part of the *Write Back Buffer* (WBB).

  - **Designer** for the R25K microprocessor. Responsible for the Load Store Unit (LSU) of the R25K, an extension of the R20K that supports L2 and L3 caches. Extended the architecture of the LSU to support L2 and L3 on-chip caches and the high-bandwidth interface, MGB-II link. Synthesized, placed and routed all the blocks of the LSU.

- 5/00 – 8/00: **Intern**, **Sun Microsystems Laboratories** (www.sunlabs.com), **Mountain View, CA, USA**. Worked with Hans Eberle on the CLINT project. Designed and implemented on Xilinx FPGA a Network Interface Card for a Cluster Interconnect which provides two separate flows for high-throughput and low-latency traffics. The NIC interfaces with a 66 MHz 64-bit PCI bus and two Gigabit transceivers. My work involved designing the architecture of the NIC and simulating it in Verilog. Used Verilog PLI and Perl to verify its functionality.

RESEARCH EXPERIENCE

- 2006 - now: **Collaborating Researcher, Telecommunication Systems Institute, Technical University of Crete, Chania, Greece** (www.tsi.gr). Main EU projects:

  - ECOSCALE - Energy-Efficient Heterogeneous Computing at Exascale, **Project Coordinator**

  - FASTCUDA - Open Source FPGA Accelerator & Hardware-Software Codesign Toolset for CUDA Kernels, Research for SMEs, **Technical Manager**

  - OSMOSIS - Open Source Modelling & Hardware Software Codesign of Embedded Systems, Research for SMEs, **Technical Manager** on behalf of TSI institute

  - VPLANET - Advanced Verification and Emulation Platform, GSRT (author, **Technical Leader**)

- 10/11 – now: **Collaborating Researcher, Computer Architecture and VLSI Systems (CARV), Foundation for Research & Technology – Hellas, Heraklio, Greece** (www.ics.forth.gr/carv). Main EU projects:

  - RAPID - Heterogeneous Secure Multi-level Remote Acceleration Service for Low-Power Integrated Systems and Devices, **Project Coordinator**

  - EUROSERVER - Green Computing Node for European micro-servers (Task Leader)

  - Encore - Enabling Technologies for a Programmable many-Core

  - HiPEAC - European Network of Excellence on High Performance and Embedded Architecture and Compilation, ICT Network of Excellence (affiliated member)

- 8/00 – 6/01: **Research Assistant, Intelligent RAM Group** (IRAM – led by Prof. David Patterson), **University of California, Berkeley, USA.** Worked on the IRAM project that integrates a vector processor and DRAM on a single chip providing high performance for media processing at low power. Main projects:

  - Designed the layout of an eight port Low Power Vector Register File consisting of two banks for Master's thesis, using layout tools from Cadence.

  - Designed and implemented in Verilog the IRAM Floating Point Unit (FPU) pipeline. Used advanced computer architecture techniques (e.g. reorder buffer with common data bus, data and structural hazard detection, value bypassing, instruction stall, kill or commit) to support out-of-order instruction execution and precise exceptions.

- 10/96 – 6/99: **Research Assistant, Computer Architecture and VLSI Group**, and **Parallel and Distributed Systems Group, Foundation for Research & Technology – Hellas, Heraklio, Greece** (www.ics.forth.gr/carv). Main projects:

  - Worked with Prof. M. Katevenis on the design of a Wormhole IP Routing Filter which is a bidirectional, 155-Mbps, FPGA-based prototype that routes and forwards IP traffic between ATM subnetworks in hardware. Simulated in Verilog and implemented on ALTERA FPGAs the core functions and port interfaces of the Filter.

  - Implemented a number of Internet tools targeted at 2-D and 3-D data processing and visualization over the Web, using various Java based GUIs, JavaScript based forms, CGI scripting in Perl 5, and VRML 2 for the 3-D data representations. Worked with Prof. S. Kapidakis for the LYDIA EU project on load balancing of high performance parallel and distributed systems.

  - Worked with Prof. E. Markatos on the Remote Memory Paging project.

PUBLICATIONS

- **JOURNALS**

  - S. Lyberis, G. Kalokerinos, M. Lygerakis, V. Papaefstathiou, I. Mavroidis, M. Katevenis, D. Pnevmatikatos, and D. S. Nikolopoulos, "FPGA Prototyping of Emerging Manycore Architectures for Parallel Programming Research using Formic Boards", *Elsevier Journal of Systems Architecture (JSA), Volume 60, Issue 6, Pages 481–493, June 2014.*

  - I. Mavroidis, I. Papaefstathiou, "Accelerating Emulation and Providing Full Chip Observability and Controllability at Run-Time", *IEEE Design & Test of Computers, Nov. 2009*, pp. 84-9.

  - M. Katevenis, Iakovos Mavroidis, G. Sapountzis, E. Kalyvianaki, Ioannis Mavroidis, G. Glykopoulos "Wormhole IP over (Connectionless) ATM" *IEEE/ACM Transactions on Networking*, vol. 9, no. 5, October 2001, pp. 650-661.

- **CONFERENCES**

  - I. Mavroidis et al, "ECOSCALE: Reconfigurable Computing and Runtime System for Future Exascale Systems", Dresden, Germany, *DATE 2016* (accepted).

  - Iakovos Mavroidis, "EUROSERVER: NUMA-like architecture for Microservers", *Margaux, France, MPSoC 2014.*

  - Yves Durand, Paul M. Carpenter, Stefano Adami, Angelos Bilas, Denis Dutoit, Alexis Farcy, Georgi Gaydadjiev, John Goodacre, Manolis Katevenis, Manolis Marazakis, Emil Matus, Iakovos Mavroidis, and John Thomson, "EUROSERVER: Energy Efficient Node for European Micro-servers", *DSD-2014.*

  - I. Mavroidis, I. Mavroidis, I. Papaefstathiou, L. Lavagno, M. Lazarescu, E. Torre, "FASTCUDA: Open Source FPGA Accelerator & Hardware-Software Codesign Toolset for CUDA Kernels" *IEEE 15th Euromicro Conference on Digital System Design (DSD 2012), Sep 5-8. Cesme, Turkey*.

  - I. Mavroidis, I. Papaefstathiou, A. Garbo, S. Nocco, J. Kim, G. Cabodi, L. Lavagno, "An Open-Source, Fast, Cost-Efficient Hardware/Software Partitioning Tool" *IEEE FCCM 2010, May 2-4, Charlotte, North Carolina.*

  - I. Mavroidis, I. Papaefstathiou, "Accelerating Hardware Simulation: Testbench Code Emulation" *IEEE International Conference on Field-Programmable Technology (ICFPT 2008), Dec 7-10, Taipei, Taiwan.*

  - I. Mavroidis, I. Papaefstathiou, "Efficient Testbench Code Synthesis for a Hardware Emulator System" *IEEE Design Automation & Test in Europe (DATE 2007), April 16-20, Nice, France.*

  - T. Orphanoudakis, G. Kornaros, I. Mavroidis, A. Nokologiannis, I. Papaefstathiou, "An Embedded Networking SoC for purely Ethernet MANs/WANs" *IEEE Symposium on Computers and Communications (ISCC'07), July 1-4, Aveiro, Portugal.*

  - I. Papaefstathiou, T. Orphanoudakis, A. Nikologiannis, G. Kornaros, I Mavroidis, "Performance evaluation of a network processor based multi-service access concentrator" 12th IEEE International Conference on Electronics, Circuits and Systems, (ICECS2005) , Dec 11-14 2005, Tunis.

  - Theofanis Orphanoudakis, Aristides Nikologiannis, Ioannis Papaefstathiou, George Kornaros, Iakovos Mavroidis, Nicholas Zervos, "Custom Network Processor Design for High-Performance Multiservice Access Concentrators", 12th International Workshop on Systems, Signals & Image Processing, 22-24 September 2005, Chalkida, Greece.

  - I. Papaefstathiou, T. Orphanoudakis, G. Kornaros, C. Kachris, I. Mavroidis, A. Nikologiannis, "Queue Management in Network Processors" IEEE Design Automation & Test in Europe (DATE 2004), March 7-11, Munich, Germany.

  - C. Kozyrakis, J. Gebis, D. Martin, S. Williams, I. Mavroidis, S. Pope, D.Jones, D. Patterson, and K. Yelick. "VIRAM: A Media-oriented vector Processor with Embedded DRAM." *Hot Chips XII Symposium, Palo Alto, CA, August 2000.*

  - Sarantos Kapidakis and Iakovos Mavroidis, "Unicode-based Digital Library Interface" *Second European Conference on Research and Advanced Technology for Digital Libraries, Crete, 21-23 Sep. 1998*

- **TECHNICAL REPORTS**

- Iakovos Mavroidis, "A Low Power 200 MHz Multiported Register File for the Vector-IRAM chip" *May 2001, TR-UCB/CSD-01-1145 of U.C. Berkeley.*

- Iakovos Mavroidis, "Hardware Implementation of a Routing Filter to support IP over ATM" *June 1999, TR-258 of ICS-FORTH*

- Sarantos Kapidakis and Iakovos Mavroidis "Multilingual Extensions to DIENST" *June 1998, TR-248 of ICS-FORTH*

HONORS & AWARDS

- **MIPS Bonus Award** stating "In Recognition of Your Outstanding Work on 20kc Debug", Feb. 2002.
- **Placed 5th in the Annual Berkeley Programming Contest 1999**. The contest was in the C programming language, and it was open to all graduate and undergraduate students.
- **University of California Regents Fellowship 1999-00.**
- Scholarships by the Greek National Scholarships Foundation (IKY) for ranking at the **top of my class in all my Undergraduate years 1995-99.**
- **Ranked at the 4th place in the 1995 National Informatics Contest and at the 6th place in the 1994 National Informatics Contest** among all Greek high-school students. Member of Greek team for International Olympiads.
  - International Olympiads: 1995 Holland (chosen but was unable to attend)
  - Balcanic Olympiads: 1995 Bulgaria, 1994 Thessaloniki - Honorable Mention
- **Honored in several National, Balcanic and International Mathematical Olympiads.** Member of Greek team for International Olympiads:
  - International Olympiads: 1995 Toronto - Honorable mention
  - Balcanic Olympiads: 1995 Sofia (chosen but was unable to attend)
  - National Olympiads : 2 Gold (1995), 2 Bronze medals (1994)
- Placed 7th in the National Physics Olympiad 1995.

TECHNICAL SKILLS SUMMARY

- Hardware Design & Verification Tools — Xilinx ISE / EDK, Mentor Graphics ModelSim, Synopsys VCS / VirSim, Cadence NCsim / SimVision / Incisive, Altera MaxPlus II, HSPice, Magic
- Hardware Languages — Verilog, VHDL
- Software Languages — Perl, Python, PHP, C/C++, CUDA, Java, HTML, CGI
- Systems, Environments — Linux, UNIX, MS Windows